Search History

STN
(HCAPLUS, INSPEC, JAPIO, USPATALL)
1/4/05

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     (FILE 'HOME' ENTERED AT 13:28:37 ON 04 JAN 2005)

     FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2' ENTERED AT 13:30:24 ON
     04 JAN 2005
L1        461836 S (SINGLE OR MONO)(8A)(CRYSTAL#)
L2           167 S (CONTROL? OR MANIPULAT? OR ALTER? OR VARY?)(8A)(OXYGEN(W)PREC
L3        383748 S (WAFER#)
L4         38940 S (CZ OR CZOCHRALSKI)
L5        133448 S (FRONT(W)SURFACE)
L6         86785 S (BACK(W)SURFACE)
L7          9353 S (CENTRAL(W)PLANE)
L8       1957254 S (DISTANCE#)
L9            45 S L7 AND(BULK(W)LAYER#)
L10         5604 S (HEAT?)(8A)(ANNEAL?(4A)TEMPERATURE#)
L11         3371 S (COOL?)(8A)(HEAT?(6A)WAFER#)
L12         6154 S (NUCLEAT?(4A)TEMPERATURE#)
L13           12 S L1 AND L2 AND L3 AND L4 AND L5 AND L6
L14            4 S L1 AND L2 AND L3 AND L4 AND L5 AND L6 AND L7 AND L8 AN

=> d l13 1-12 abs,bib

L13  ANSWER 1 OF 12  USPATFULL on STN
AB     The present invention is directed to a single crystal
       Czochralski-type silicon wafer, and a process for the
       preparation thereof, which has a non-uniform distribution of crystal
       lattice vacancies therein, the peak concentration being present in the
       wafer bulk between an imaginary central plane and a surface of
       the wafer, such that, upon being subjected to the heat
       treatment cycles of essentially any arbitrary electronic device
       manufacturing process, the wafer forms oxygen precipitates in
       the wafer bulk and a thin or shallow precipitate-free zone
       near the wafer surface.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN     2003:274457  USPATFULL
TI     Process for controlling denuded zone depth in an ideal
       oxygen precipitating silicon wafer
IN     Libbert, Jeffrey L., O'Fallon, MO, UNITED STATES
       Binns, Martin Jeffrey, St. Charles, MO, UNITED STATES
       Falster, Robert J., London, UNITED KINGDOM
PA     MEMC Electronic Materials, Inc. (U.S. corporation)
PI     US 2003192469      A1   20031016
AI     US 2002-277660     A1   20021022 (10)
PRAI   US 2002-371324P     20020410 (60)
DT     Utility
FS     APPLICATION
LREP   SENNIGER POWERS LEAVITT AND ROEDEL, ONE METROPOLITAN SQUARE, 16TH FLOOR,
       ST LOUIS, MO, 63102
CLMN   Number of Claims: 69
ECL    Exemplary Claim: 1
DRWN   2 Drawing Page(s)
LN.CNT 1266
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L13  ANSWER 2 OF 12  USPATFULL on STN
AB     A silicon wafer having a controlled oxygen
       precipitation behavior such that a denuded zone extending inward
       from the front surface and oxygen precipitates in
       the wafer bulk sufficient for intrinsic gettering purposes are
       ultimately formed. Specifically, prior to formation of the oxygen
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precipitates, the **wafer** bulk comprises dopant stabilized oxygen precipitate nucleation centers. The dopant is selected from a group consisting of nitrogen and carbon and the concentration of the dopant is sufficient to allow the oxygen precipitate nucleation centers to withstand thermal processing such as an epitaxial deposition process while maintaining the ability to dissolve any grown-in nucleation centers.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:198981 USPATFULL
TI Ideal oxygen precipitating silicon **wafers** with nitrogen/carbon stabilized oxygen precipitate nucleation centers and process for making the same
IN Mule'Stagno, Luciano, St. Louis, MO, UNITED STATES
Libbert, Jeffrey L., O'Fallon, MO, UNITED STATES
Phillips, Richard J., St. Peters, MO, UNITED STATES
Kulkarni, Milind, St. Louis, MO, UNITED STATES
Banan, Mohsen, Grover, MO, UNITED STATES
Brunkhorst, Stephen J., Chesterfield, MO, UNITED STATES
PA MEMC Electronic Materials, Inc. (U.S. corporation)
PI US 2003136961 A1 20030724
US 6808781 B2 20041026
AI US 2002-328481 A1 20021223 (10)
PRAI US 2001-345191P 20011221 (60)
US 2001-345178P 20011221 (60)
DT Utility
FS APPLICATION
LREP SENNIGER POWERS LEAVITT AND ROEDEL, ONE METROPOLITAN SQUARE, 16TH FLOOR, ST LOUIS, MO, 63102
CLMN Number of Claims: 45
ECL Exemplary Claim: 1
DRWN 1 Drawing Page(s)
LN.CNT 1247
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L13 ANSWER 3 OF 12 USPATFULL on STN
AB The present invention is directed to a **single crystal Czochralski**-type silicon **wafer**, and a process for the preparation thereof, which has at least a surface layer of high resistivity, the layer having an interstitial oxygen content which renders it incapable of forming thermal donors in an amount sufficient to affect resistivity upon being subjected to a conventional semiconductor device manufacturing process. The present invention further directed to a silicon on insulator structure derived from such a **wafer**.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:78718 USPATFULL
TI Control of thermal donor formation in high resistivity **CZ** silicon
IN Binns, Martin Jeffrey, St. Charles, MO, UNITED STATES
Falster, Robert J., London, UNITED KINGDOM
Libbert, Jeffrey L., O'Fallon, MO, UNITED STATES
PA MEMC Electronic Materials, Inc. (U.S. corporation)
PI US 2003054641 A1 20030320
AI US 2002-120714 A1 20020411 (10)
PRAI US 2001-283103P 20010411 (60)
US 2001-300364P 20010622 (60)
US 2002-371324P 20020410 (60)
DT Utility
FS APPLICATION
LREP SENNIGER POWERS LEAVITT AND ROEDEL, ONE METROPOLITAN SQUARE, 16TH FLOOR, ST LOUIS, MO, 63102

CLMN Number of Claims: 62
ECL Exemplary Claim: 1
DRWN 2 Drawing Page(s)
LN.CNT 1585
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L13 ANSWER 4 OF 12 USPATFULL on STN
AB The present invention is directed to a process for producing a silicon on insulator (SOI) structure having intrinsic gettering, wherein a silicon substrate is subjected to an ideal precipitating **wafer** heat treatment which enables the substrate, during the heat treatment cycles of essentially any arbitrary electronic device manufacturing process to form an ideal, non-uniform depth distribution of oxygen precipitates, and wherein a dielectric layer is formed beneath the surface of the **wafer** by implanting oxygen or nitrogen ions, or molecular oxygen, beneath the surface and annealing the **wafer**. Additionally, the silicon **wafer** may initially include an epitaxial layer, or an epitaxial layer may be deposited on the substrate during the process of the present invention.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:10739 USPATFULL
TI Process for producing silicon on insulator structure having intrinsic gettering by ion implantation
IN Falster, Robert J., London, UNITED KINGDOM
Libbert, Jeffrey L., O' Fallon, MO, UNITED STATES
PA MEMC Electronic Materials, Inc. (non-U.S. corporation)
PI US 2003008435 A1 20030109
AI US 2002-177444 A1 20020621 (10)
PRAI US 2001-300208P 20010622 (60)
US 2001-337623P 20011205 (60)
DT Utility
FS APPLICATION
LREP SENNIGER POWERS LEAVITT AND ROEDEL, ONE METROPOLITAN SQUARE, 16TH FLOOR, ST LOUIS, MO, 63102
CLMN Number of Claims: 76
ECL Exemplary Claim: 1
DRWN 12 Drawing Page(s)
LN.CNT 2242
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L13 ANSWER 5 OF 12 USPATFULL on STN
AB The process relates to a process for nucleating and growing oxygen precipitates in a silicon **wafer**. The process includes subjecting a **wafer** having a non-uniform concentration of crystal lattice vacancies with the concentration of vacancies in the bulk layer being greater than the concentration of vacancies in the surface layer to a non-isothermal heat treatment to form of a denuded zone in the surface layer and to cause the formation and stabilization of oxygen precipitates having an effective radial size 0.5 nm to 30 nm in the bulk layer. The process optionally includes subjecting the stabilized **wafer** to a high temperature thermal process (e.g. epitaxial deposition, rapid thermal oxidation, rapid thermal nitridation and etc.) at temperatures in the range of 1000° C. to 1275° C. without causing the dissolution of the stabilized oxygen precipitates.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:318887 USPATFULL
TI Method for the preparation of a semiconductor substrate with a non-uniform distribution of stabilized oxygen precipitates
IN Borgini, Marco, Borgo Vercelli, ITALY
Gambaro, Daniela, Galliáte, ITALY

Ravani, Marco, Novara, ITALY
Ries, Michael J., St. Charles, MO, UNITED STATES
Sacchetti, Laura, Milano, ITALY
Standley, Robert W., Chesterfield, MO, UNITED STATES
Falster, Robert J., London, UNITED KINGDOM
Stinson, Mark G., East Alton, IL, UNITED STATES
PA MEMC Electronic Materials, Inc. (non-U.S. corporation)
PI US 2002179006 A1 20021205
AI US 2002-127509 A1 20020422 (10)
PRAI US 2001-285180P 20010420 (60)
US 2001-345165P 20011221 (60)
DT Utility
FS APPLICATION
LREP SENNIGER POWERS LEAVITT AND ROEDEL, ONE METROPOLITAN SQUARE, 16TH FLOOR, ST LOUIS, MO, 63102
CLMN Number of Claims: 54
ECL Exemplary Claim: 1
DRWN 3 Drawing Page(s)
LN.CNT 1425
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L13 ANSWER 6 OF 12 USPATFULL on STN
AB A process for heat-treating a **single crystal** silicon **wafer** to dissolve agglomerated vacancy defects and to influence the precipitation behavior of oxygen in the **wafer** in a subsequent thermal processing step is disclosed. The **wafer** has a **front surface**, a **back surface**, and a central plane between the front and back surfaces. In the process, the **wafer** is subjected to a thermal anneal to dissolve agglomerated vacancy defects present in a stratum extending from the **front surface** toward the center of the **wafer** . The annealed **wafer** is then heat-treated to form crystal lattice vacancies, the vacancies being formed in the bulk of the silicon. The heat-treated **wafer** is cooled from the temperature of said heat treatment at a rate which allows some, but not all, of the crystal lattice vacancies to diffuse to the **front surface** to produce a **wafer** having a vacancy concentration profile in which the peak density is at or near the central plane with the concentration generally decreasing in the direction of the **front surface** of the **wafer** .

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:305538 USPATFULL
TI Process for producing thermally annealed **wafers** having improved internal gettering
IN Falster, Robert J., London, UNITED KINGDOM
Binns, Martin Jeffrey, St. Charles, MO, UNITED STATES
Korb, Harold W., Town ?amp; Country, MO, UNITED STATES
PA MEMC Electronic Materials, Inc.
PI US 2002170631 A1 20021121
US 6686260 B2 20040203
AI US 2002-67070 A1 20020204 (10)
RLI Division of Ser. No. US 1999-385108, filed on 27 Aug 1999, GRANTED, Pat. No. US 6361619
PRAI US 1998-98921P 19980902 (60)
DT Utility
FS APPLICATION
LREP SENNIGER POWERS LEAVITT AND ROEDEL, ONE METROPOLITAN SQUARE, 16TH FLOOR, ST LOUIS, MO, 63102
CLMN Number of Claims: 55
ECL Exemplary Claim: 1
DRWN 13 Drawing Page(s)

LN.CNT 1320
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L13 ANSWER 7 OF 12 USPATFULL on STN
AB A **single crystal** silicon **wafer** comprising a **front surface**, a **back surface**, a lateral surface joining the front and back surfaces, a central axis perpendicular to the front and back surfaces, and a segment which is axially symmetric about the central axis extending substantially from the **front surface** to the **back surface** in which crystal lattice vacancies are the predominant intrinsic point defect, the segment having a radial width of at least about 25% of the radius and containing agglomerated vacancy defects and a residual concentration of crystal lattice vacancies wherein (i) the agglomerated vacancy defects have a radius of less than about 70 nm and (ii) the residual concentration of crystal lattice vacancy intrinsic point defects is less than the threshold concentration at which uncontrolled oxygen precipitation occurs upon subjecting the **wafer** to an oxygen precipitation heat treatment.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:226110 USPATFULL
TI Process for preparing **single crystal** silicon having improved gate oxide integrity
IN Falster, Robert J., London, UNITED KINGDOM
Voronkov, Vladimir V., Merano, ITALY
Mutti, Paolo, Milan, ITALY
Bonoli, Fancesco, Novara, ITALY
PA MEMC Electronic Materials, Inc. (non-U.S. corporation)
PI US 2002121238 A1 20020905
AI US 2002-39196 A1 20020102 (10)
PRAI US 2001-259362P 20010102 (60)
DT Utility
FS APPLICATION
LREP SENNIGER POWERS LEAVITT AND ROEDEL, ONE METROPOLITAN SQUARE, 16TH FLOOR, ST LOUIS, MO, 63102
CLMN Number of Claims: 59
ECL Exemplary Claim: 1
DRWN 17 Drawing Page(s)
LN.CNT 1985
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L13 ANSWER 8 OF 12 USPATFULL on STN
AB A process for heat-treating a **single crystal** silicon **wafer** to dissolve agglomerated vacancy defects and to influence the precipitation behavior of oxygen in the **wafer** in a subsequent thermal processing step is disclosed. The **wafer** has a **front surface**, a **back surface**, and a central plane between the front and back surfaces. In the process, the **wafer** is subjected to a thermal anneal to dissolve agglomerated vacancy defects present in a stratum extending from the **front surface** toward the center of the **wafer**. The annealed **wafer** is then heat-treated to form crystal lattice vacancies, the vacancies being formed in the bulk of the silicon. The heat-treated **wafer** is cooled from the temperature of said heat treatment at a rate which allows some, but not all, of the crystal lattice vacancies to diffuse to the **front surface** to produce a **wafer** having a vacancy concentration profile in which the peak density is at or near the central plane with the concentration generally decreasing in the direction of the **front surface** of the **wafer**.

AN 2002:63396 USPATFULL
TI Thermally annealed **wafers** having improved internal gettering
IN Falster, Robert J., Milan, ITALY
Binns, Martin Jeffrey, St. Charles, MO, United States
Korb, Harold W., Town & Country, MO, United States
PA MEMC Electronic Materials, Inc., St. Peters, MO, United States (U.S. corporation)
PI US 6361619 B1 20020326
AI US 1999-385108 19990827 (9)
PRAI US 1998-98921P 19980902 (60)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Chaudhuri, Olik; Assistant Examiner: Peratta, Ginette
LREP Senniger, Powers, Leavitt & Roedel
CLMN Number of Claims: 25
ECL Exemplary Claim: 1
DRWN 16 Drawing Figure(s); 13 Drawing Page(s)
LN.CNT 1194

L13 ANSWER 9 OF 12 USPATFULL on STN
AB A method of manufacturing a silicon **wafer** with robust gettering sites and a low concentration of surface defects is provided. The method comprises adding polycrystalline silicon to a crucible; adding a nitrogen-containing dopant to the crucible; heating the crucible to form a nitrogen-doped silicon melt; pulling a silicon crystal from the melt according to the **Czochralski** technique; forming a silicon **wafer** from the silicon crystal, wherein the silicon **wafer** includes a **front surface** and a **back surface**; placing the silicon **wafer** into a deposition chamber; heating the **wafer**; and simultaneously depositing an epitaxial first film of a desired compound onto the **front surface** of the **wafer** and a second film of the desired compound onto the **back surface** of the **wafer**.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:138132 USPATFULL
TI Optimized silicon **wafer** gettering for advanced semiconductor devices
IN Dietze, Gerald R., Portland, OR, United States
Hanna, Sean G., Portland, OR, United States
Radzimski, Zbigniew J., Brush Prairie, WA, United States
PI US 2001015168 A1 20010823
US 6632277 B2 20031014
AI US 2001-759028 A1 20010111 (9)
RLI Continuation-in-part of Ser. No. US 2000-567659, filed on 9 May 2000, PENDING Continuation-in-part of Ser. No. US 1999-353196, filed on 14 Jul 1999, PENDING Continuation-in-part of Ser. No. US 1999-353197, filed on 14 Jul 1999, PENDING
DT Utility
FS APPLICATION
LREP KOLISCH HARTWELL DICKINSON MCCORMACK & H, EUSER, 520 S.W. YAMHILL STREET, SUITE 200, PORTLAND, OR, 97204
CLMN Number of Claims: 23
ECL Exemplary Claim: 1
DRWN 3 Drawing Page(s)
LN.CNT 729
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L13 ANSWER 10 OF 12 USPATFULL on STN
AB A process for the preparation of silicon **wafers** having a non-uniform distribution of **oxygen precipitate** nucleation centers. Silicon **wafers** having a **controlled**

distribution of **oxygen precipitate** nucleation centers are prepared by heating the **wafer** in a manner to create a temperature gradient across the thickness of the **wafer** for a period of time. Upon a subsequent oxygen precipitation heat treatment, those regions of the **wafer** which were rapidly heated to a temperature in excess of about 900° C. will form a denuded zone whereas those regions of the **wafer** which did not achieve a temperature in excess of about 900° C. during the rapid heating will form oxygen precipitates.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 1999:33895 USPATFULL
TI Process for the preparation of silicon **wafers** having a **controlled** distribution of **oxygen precipitate** nucleation centers
IN Falster, Robert, Milan, Italy
PA MEMC Electronic Materials, Inc., St. Peters, MO, United States (U.S. corporation)
PI US 5882989 19990316
AI US 1997-934946 19970922 (8)
DT Utility
FS Granted
EXNAM Primary Examiner: Bowers, Charles; Assistant Examiner: Christianson, Keith
LREP Senniger, Powers, Leavitt & Roedel
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 5 Drawing Figure(s); 2 Drawing Page(s)
LN.CNT 366
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L13 ANSWER 11 OF 12 USPAT2 on STN
AB A silicon **wafer** having a **controlled oxygen precipitation** behavior such that a denuded zone extending inward from the **front surface** and oxygen precipitates in the **wafer** bulk sufficient for intrinsic gettering purposes are ultimately formed. Specifically, prior to formation of the oxygen precipitates, the **wafer** bulk comprises dopant stabilized oxygen precipitate nucleation centers. The dopant is selected from a group consisting of nitrogen and carbon and the concentration of the dopant is sufficient to allow the oxygen precipitate nucleation centers to withstand thermal processing such as an epitaxial deposition process while maintaining the ability to dissolve any grown-in nucleation centers.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:198981 USPAT2
TI Silicon **wafers** with stabilized oxygen precipitate nucleation centers and process for making the same
IN Mule'Stagno, Luciano, St. Louis, MO, United States
Libbert, Jeffrey L., O'Fallon, MO, United States
Phillips, Richard J., St. Peters, MO, United States
Kulkarni, Milind, St. Louis, MO, United States
Banan, Mohsen, Grover, MO, United States
Brunkhorst, Stephen J., Chesterfield, MO, United States
PA MEMC Electronic Materials, Inc., St. Peters, MO, United States (U.S. corporation)
PI US 6808781 B2 20041026
AI US 2002-328481 20021223 (10)
PRAI US 2001-345178P 20011221 (60)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Stein, Stephen

LREP Senniger Powers
CLMN Number of Claims: 48
ECL Exemplary Claim: 1
DRWN 1 Drawing Figure(s); 1 Drawing Page(s)
LN.CNT 1268
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L13 ANSWER 12 OF 12 USPAT2 on STN
AB A process for heat-treating a **single crystal** silicon **wafer** to dissolve agglomerated vacancy defects and to influence the precipitation behavior of oxygen in the **wafer** in a subsequent thermal processing step. The process includes subjecting the **wafer** to a heat treatment to dissolve agglomerated vacancy defects, rapid thermally annealing the heat-treated **wafer** to cause the formation of crystal lattice vacancies throughout the **wafer** and controlling the cooling rate of the annealed **wafer** to allow some, but not all, of the crystal lattice vacancies to diffuse to the **front surface** to produce a **wafer** having a nonuniform vacancy concentration with the concentration of vacancies in the bulk of the **wafer** being greater than the concentration in the surface layer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:305538 USPAT2
TI Process for producing thermally annealed **wafers** having improved internal gettering
IN Falster, Robert J., London, UNITED KINGDOM
Binns, Martin Jeffrey, St. Charles, MO, United States
Korb, Harold W., Town & Country, MO, United States
PA MEMC Electronics Materials, Inc., St. Peters, MO, United States (U.S. corporation)
PI US 6686260 B2 20040203
AI US 2002-67070 20020204 (10)
RLI Division of Ser. No. US 1999-385108, filed on 27 Aug 1999, now patented, Pat. No. US 6361619
PRAI US 1998-98921P 19980902 (60)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Fahmy, Wael; Assistant Examiner: Peralta, Ginette
LREP Senniger, Powers, Leavitt & Roedel
CLMN Number of Claims: 30
ECL Exemplary Claim: 1
DRWN 16 Drawing Figure(s); 13 Drawing Page(s)
LN.CNT 1262
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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